EUROPEAN COMMISSION

**Thematic Priority:**
SIXTH FRAMEWORK PROGRAM

**Priority 2.5.3**
INFORMATION SOCIETY TECHNOLOGIES
**Unit G3 Embedded Systems**


**Project Acronym:**

**SOCRADES**

**Project Full Title:**

**Service-Oriented Cross-layer infRAstructure for Distributed smart Embedded devices**

**Proposal/Contract No: EU FP6 IST-5-034116 IP SOCRADES**

# Deliverable D5.6.4

# Cost Analysis of Proposed µGateway

| | |
|---|---|
| **Status:** | **Final** |
| **Version:** | **V1.0**[1] |
| **Dissemination Level**[2]**:** | **CONFIDENTIAL** |
| **Date:** | **29.05.2009** |

Organization Name of the Lead Contractor for this Deliverable**: ARM**

[1] V0.x before peer-review approval, V1.0 at the approval, V1.x minor revisions, V2.0 major revision
[2] See Annex A for explanation of Dissemination Levels, as defined in the DoW

## Status Description:

| | | | |
|---|---|---|---|
| Scheduled completion date[3]: | 30.04.2009 | Actual completion date[4]: | 29.05.2009 |
| Short document description: | Deliverable D5.6.2 describes the purpose and activities of a project that has the objective of creating a microcontroller with DSP and SIMD capabilities with focus on character data processing. | | |
| Author(s) deliverable: | Paul Marston, Jürgen Jagst (ARM/ARM) | **Report/deliverable classification:**<br>[x] Deliverable<br>[ ] Three-Monthly Activity Report<br>[ ] Six-Monthly Activity Report | |

| Partner (Contributions / Peer reviews) | | |
|---|---|---|
| [x] [x] Schneider Electric Automation | [ ] [x] Loughborough University | |
| [ ] [x] ABB | [ ] [x] Luleå University of Technology | |
| [ ] [x] APS GmbH | [ ] [x] Politecnico di Milano | |
| [ ] [ ] Boliden AB | [ ] [x] SAP AG | |
| [ ] [ ] FlexLink Automation Oy. | [ ] [x] Siemens AG | |
| [ ] [x] Institut f. Automation und Kommunikation e.V. Magdeburg | [ ] [x] Tampere University of Technology | |
| [ ] [ ] Kungliga Tekniska Högskolan | [ ] [ ] Jaguar Cars Ltd. | |
| | [x] [x] ARM Ltd. | |
| | [x] [x] Schneider Electric Industries | |

| | | | |
|---|---|---|---|
| Peer review approval : | [x] Approved<br>[ ] Rejected (improve as specified hereunder) | Date: | 27.05.2009 |
| Suggested improvements: | | | |

## Version History:

| Version: | Date: | Comments, Changes, Status: | Person(s)[5]: |
|---|---|---|---|
| 0.5 | 12.05.2009 | Feedback session inputs. Layout improvement | ARM/JJ |
| 0.4 | 08.05.2009 | Feedback session inputs. Added chapter 2.2 | ARM/JJ |
| 0.3 | 29.04.2009 | Feedback session inputs. Replace Merlin by Cortex-M3 description, added 4.2.1-4.2.3 | ARM/JJ |
| 0.2 | 17.04.2009 | Added detailed silicon estimations from model. Typo fixing and minor rephrasing | ARM/JJ |
| 0.1 | 06.04.2009 | Draft revision | ARM/JJ |

[3] As defined in the DoW
[4] Scheduled date for approval
[5] A list of company short tags can be found in DoW

# Table of Contents:



# List of Figures:



# List of Tables:

## Dissemination Level:

| | |
|---|---|
| PU | Public |
| PP | Restricted to other programme participants (including the Commission Services) |
| RE | Restricted to a group specified by the consortium (including the Commission |
| CO | Confidential, only for members of the consortium (including the Commission Services) |

# 1. Introduction

The evaluation prototype hardware has been realized in an FPGA-based solution on a coustomized evaluation board hardware. This is very useful during debugging and implementation phase due to low cost & effort for required hardware changes in functionality. Additionally several I/O interfaces can be implemented according to requirements of the application space in industrial networking and an e.g. independent BLDC-motor controller.

For volume production an ASIC-based silicon solution is the far better solution due to usually higher performance figures and reduced cost for production volume due to specialized silicon of certain functionality on a smaller silicon-die size.

This report shall give an overview for a silicon cost-estimation based on selected functionality for an industrial uGateway controller and detailed information on main cost-driving factors and proposal for dedicated cost savings. For this deliverable document some estimation has been made based on today silicon technology and its availability.

# 2. Architectural and Design

## 2.1. Motivation

The evaluation prototype hardware shall be transferred from a FPGA based solution into an ASIC for high volume production to lower cost for implementations in the industrial networking field. Especially small sensors and actuators are under price pressure due to frequency of occurrence in industrial installations for a certain industrial functionality and facility.

## 2.2. New Capabilities for Industrial Computing

The MCU core called 'Merlin' will will be the first solution for small embedded industrial networking solutions which introduces several new computing functionality derived from high performance computing solutions into low cost MCUs. Those functionalities are:

Single Instruction Multiple Data (SIMD) to improve MCU networking stack processing

DSP functionality to improve complex software algorithms

Floating point support for Modeling Tool interaction

All new functionality is intended to improve operation of software (e.g. DPWS) on industrial hardware implementations as well as reducing cost by integrating external functionality on one single die and silicon chip for the very first time.

## 2.3. MCU Core Functional Overview

MCU core of a processor for the evaluation prototype hardware exists with with the following top level structure. Further I/O interfaces required for the evaluation prototype hardware realisation will be included in chapter 3.2 (but seem to be less important cost factors).

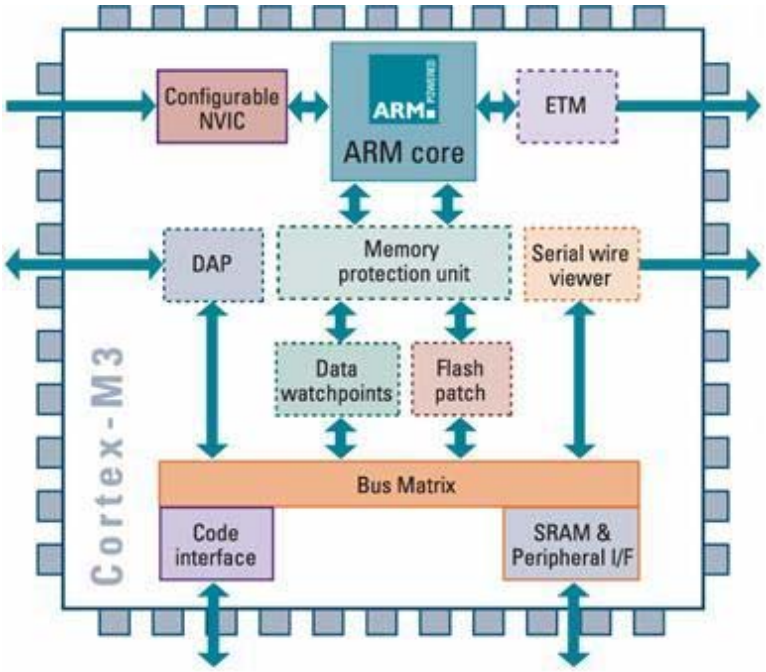


**Figure 1: Abstract top level block diagram of Cortex-M3 MCU**

### *2.4. Main MCU Core Components*

The main components of the Cortex-M3 MCU, as identified in Figure 1 are outlined below.

**ARM core –** The central processing unit, or processor core, controls the flow of instruction execution and data processing.

**Bus Matrix** - Instruction and data memory is external to the MCU. The bus matrix arbitrates the flow of data from memory and peripheral components, as determined by the CPU.

**Memory Protection Unit** - The MPU ensures that accesses to the defined regions of external memories and peripherals are valid.

**Flash Patch** - The Flash Patch component provides the ability to replace erroneous code in the fixed instruction ROM with corrected code in changeable memory such as RAM or Flash ROM.

**DAP** - The Debug Access Port provides and controls access to the MCU memories and registers for debugging purposes. An external debugging tool communicates with the DAP via a serial debug interface.

**ETM** - The Embedded Trace Macro cell provides a stream of information at real-time, that allows the instruction execution flow of the MCU to be monitored externally.

**Data Watch points** - This component, under debug control, monitors data transfers for specified data items. Upon detection of such data during program execution, this block triggers or halts trace execution by the ETM.

**Serial Wire Viewer** - This component formats trace information from the ETM as standard ASCII data, sent serially to trace analysis tools through a single pin.

**NVIC** - The Nested Vectored Interrupt Controller provides a configurable number of interrupts to the MCU, with selectable priority levels. This allows high speed transfer from normal code execution to an Interrupt Service Routine (ISR), and from one ISR to another of higher priority.

**Code bus -** 2x AHB-Lite buses for instruction code bus and data8Coefficient code bus

**SRAM & Peripheral IF** Peripheral bus interfaces for internal SRAM and slow I/O interfaces

### 2.5. I/O Interfaces

For the evaluation prototype hardware a typical Industrial I/O interface variety has be selected like Ethernet, BLDC-Motor controller, Pulse-width-modulation (PWM), SPI, general purpose IO (GPIO) and common glue logic like reset and clock distribution as well as internal standard bus systems for interconnection purposes.

# 3. Silicon Size Calculation

## 3.1. Silicon Area Consumption

The calculation is split into two major groups, the gate count and the known length and width of an e.g. memory area in a certain silicon technology. **Note:** This is only an example implementation for illustration considering major required I/O interfaces combined with a huge storage capacity.

## 3.2. The Silicon Die Size Estimation

The table below shows a typical estimation for an evaluation prototype hardware including ECU core and main peripheral components.

| Module | Gate count | Length (um) | Width (um) | Area (mm2) |
|---|---|---|---|---|
| Cortex-M3 (CM3) | 60.000 | | | 0 |
| JTAG Interface (Part of CM3) | | | | 0 |
| 16-input Interrupt Controller (Part of CM3) | | | | 0 |
| 1M SRAM | | 8000 | 5780 | 46,24 |
| 2M Flash Memory | | 7440 | 4460 | 33,18 |
| Memory Interface Unit (PL241) | 32.000 | | | 0 |
| 2x 16-bit timer | 4.200 | | | 0 |
| 32-bit watchdog timer | 1.465 | | | 0 |
| GPIO (PL061) | 1.800 | | | 0 |
| SPI (PL022) | 7.500 | | | 0 |
| AHB (Bridge) | 400 | | | 0 |
| APB (Bridge) | 3.600 | | | 0 |
| Power-on-reset | | 387 | 387 | 0,14 |
| Power Controller | | 500 | 500 | 0,25 |
| Clock Synthesizer 60-300MHz PLL | 3.000 | | | 0 |
| PWM | 2.300 | | | 0 |
| 8-channel 10-bit ADC | | 435 | 435 | 0,18 |
| SCI | | | | 0 |
| 802.15.4 (Zigbee) | | | | 0 |
| CAN2.0C (found 2.0B) | 6.500 | | | 0 |
| 4-channel analoge Output | | | | 0 |
| Ethernet 10/100 | 7.000 | | | 0 |
| **Totals** | 129.765 | | | 80,01 |

| **Calculate die Size required for prototype** | | |
|---|---|---|
| Assuming a cell density of | 120 | Kgates/mm2 |
| The total Gate Count of | 129.765 | Gates |
| Will occupy an Area of | 1,08 | mm2 |
| Added to the calculated area of | 80,01 | mm2 |
| Gives a total logic area of | 81,09 | mm2 |
| | | |
| Assuming a utilisation of | 70 | % |
| Required die size will be | 115,84 | mm2 |

**Table 1: Silicon Die Size Estimation**

### *3.3. The Major Die Size Consumption*

As seen from the estimated table above the major silicon area consumption is caused by SRAM or FLASH memory.. The 1 MByte SRAM area is bigger than the 2MByte FLASH memory due to its internal structure. Below there will be a short explanation how this is physically caused by technological implementations.

#### 3.3.1. *SRAM Memory*

Usually a standard SRAM memory it is built of 6 field-effect transistors. The graphic below may illustrate the principle of a single SRAM cell which stores a single bit-information.

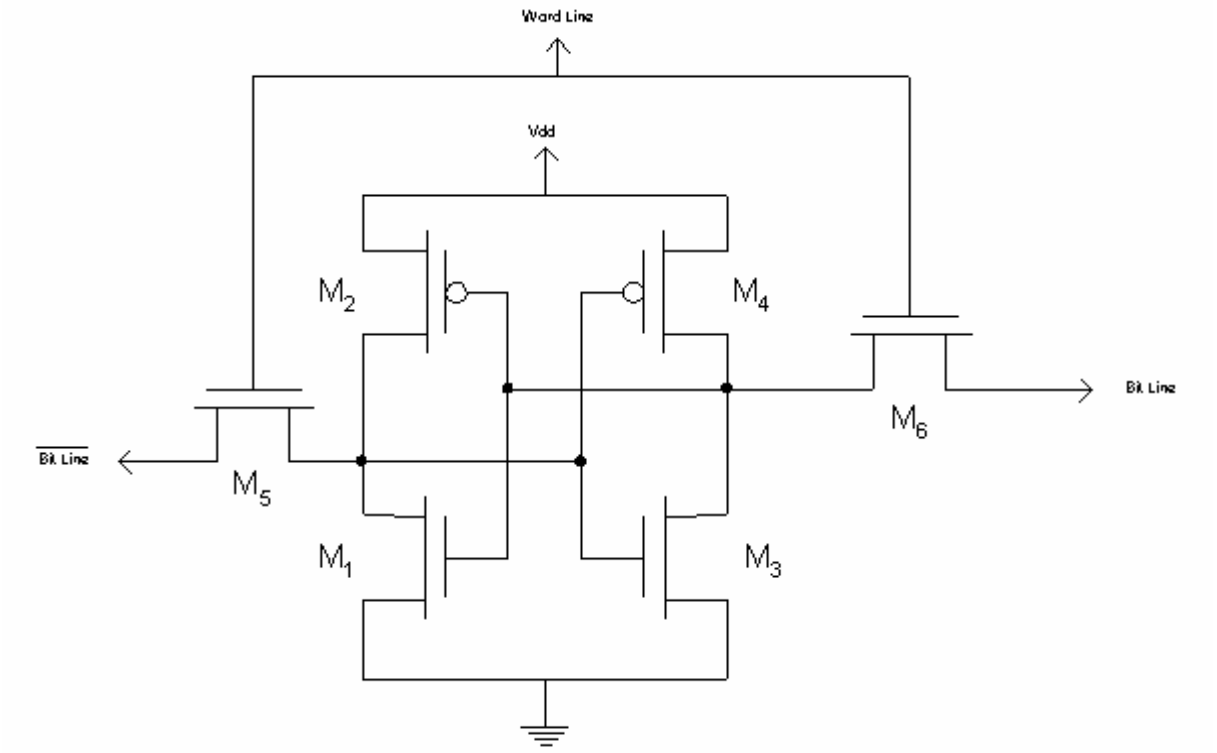


**Figure 2: 6T- SRAM Cell (source: www.cedcc.psu.edu)**

SRAM memory cell dimensions are directly dependent on the technology of the silicon manufacturer which will be used for the evaluation prototype hardware ASIC implementation.

#### 3.3.2. *FLASH Memory*

The structure of a FLASH memory cell is not as easy to describe, because there are two major implementations on the market the fast NOR-FLASH memory technology and a smaller but slower and more reliable NAND-FLASH memory. Additionally there are single level cells (SLC) and multi level cells (MLC) technologies on the market which store one ore more physical bits per cell or unit. But as an overall assumption it can be said that a FLASH memory bit cell is built of one special field effect transistor which consumes less silicon die size than a SRAM memory cell. But it is implementation specific which silicon technology is used by silicon manufacturer for the evaluation prototype hardware ASIC implementation of FLASH memory storage.

### 3.4. The Assumption …

As seen from chapters 3.2 and 3.3 above the major silicon die area consumption is caused by SRAM or FLASH memory. Therefore the functional elements like peripheral I/O or CPU core etc. can be disregarded in further cost and die size estimations. The dominating memory size requirements will be the cost driver, regardless if SRAM-memory or FLASH-memory technology is used.

### 3.5. The Silicon Companies Business …

Today's silicon manufacturers have to operate on good profit levels to burden cost for running large manufacturing plants and factories. So the production cost of a evaluation prototype hardware can only be estimated to be around half of the selling price to silicon manufacturers customers e.g. distributors. But this estimation is very weak not considering business relationships and purchased volume over time as well as silicon technology used for the evaluation prototype hardware ASIC.

## 4. Cost Estimation & Possible Savings

### 4.1. Estimation of Die Cost

A cost estimation models from common processes from an famous Automotive silicon manufacturer shows cost of around 3-5 US-Dollar per silicon die assuming a 90nm process on 300mm wafers for 1MByte SRAM and 2MByte FLASH memory. Additionally a cost adder of about ~0,50 US-Dollar for additional efforts like packaging, number of pins and testing effort shall be considered. All estimations are based on a year 2008 model, see [12]. The production cost will decease in a double digit percentage for year 2009 and stabilizes over the year in the future on that level [12].

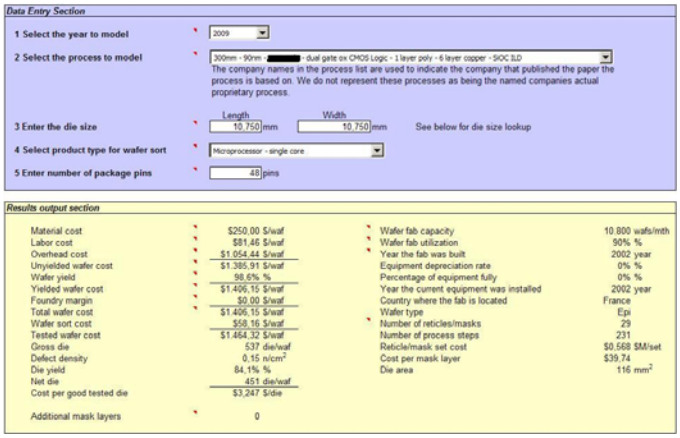


**Figure 3: Cost Estimation Example (Max. Memory)**

Please note that this is rough cost estimation for the evaluation prototype hardware not considering side effects like special supplier relations, application requirements (e.g. special packaging requirements for high temperature environments), volume production numbers and political stability.

### 4.2. Cost Saving Opportunities

#### 4.2.1. Memory Storage Variants

Due to the fact that SRAM-memory and FLASH-memory consume the majority of the silicon die size, a reduction of memory requirements will dramatically reduce production cost per die.

For example a 50% reduction of the die size from around 116mm^2 to 58mm^2 will reduce the silicon die size cost of about 55% in 2008 with an outlook to shrink down to ~25% in 2015. General conditions for the numbers as mentioned before are extremely dependent on technology framework [12].

As a consequence, storage space in SRAM-memory and FLASH-memory used by software implementation solution has a direct impact on evaluation prototype hardware ASIC cost. It is recommended that highly size-optimized software shall be used to run an application; it has direct impact in the cost and cost-savings.

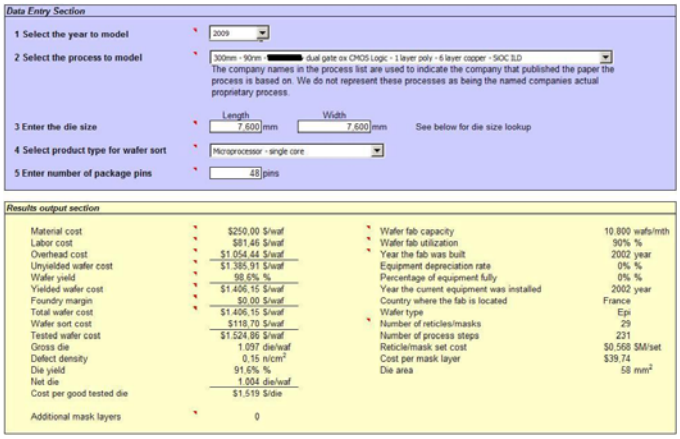


**Figure 4: Cost Savings Example (Smaller Memory)**

### 4.2.2. *Core Substitution Efficiency*

Besides the memory variants, the gate count for the evaluation prototype hardware can be further reduced by replacing the Cortex-M3 MCU with a Cortex-M0 MCU. The Cortex-M0 provides a slightly lower performance for sensor/actuator application processing but a drastically reduced gate count of about ~12K gates (=-80%) on a lower power consumption level but it maintains full software code compatibility at the same time.

Additionally this may be beneficial in cases of Automotive requirements or Analog and even Mixed-Signal solutions for e.g. integrated physical sensors which may require larger gate geometries due to the use-case and therefore larger die sizes in some implementation cases which drives into higher cost issues.

### 4.2.3. *Instruction Set Capabilities*

As mentioned in [12] the application software implementation of the evaluation prototype hardware can be improved by using a hardware SIMD-instruction set implementation which helps to speedup code execution on one hand and reduces size of the application code executable on the other hand.

Especially in the case where the hardware geometry can physically shrink to smaller geometries in advanced silicon technologies without affecting the functionality of the ASIC (e.g. no pad limitations), instruction set support for efficient software generation might be helpful to consume even less memory as well. SIMD instructions provide much more flexibility to the code compiler to optimize and profile e.g. certain software algorithms by replacing large software library functions with instructions built in hardware (e.g. instructions for matrix multiplication etc.).

# 5. References

## *5.1. Input Documents*

[1]
Cortex-M3 Engineering Specification (confidential), 2008, ARM Limited, Cambridge, UK

[2]
ARMv7M Architecture Reference Manual, 2006-2008, ARM Limited, Cambridge, UK

[3]
ARMv7M Extensions Proposal (confidential) , 2008, ARM Limited, Cambridge, UK

[4]
ARM Information Center, ARM966-E Technical Reference Manual, 2008, ARM Limited, Cambridge, UK

[5]
ARM Information Center, ARM Cortex-M3 Technical Reference Manual, 2008, ARM Limited, Cambridge, UK

[6]
ARM Information Center, ARM RealView™ Development Suite, 2006-2008, ARM Limited, Cambridge, UK

[7]
ARM Information Center, Keil™ Embedded Development, 2007-2008, ARM Limited, Cambridge, UK

[8]
Application Note: Using the ARM Cortex-M3 on the Microcontroller Prototyping System, 2006-2008, ARM Limited, Cambridge, UK

[9]
Information on FLASH memory implementation and related constraints, 2009, http://en.wikipedia.org/wiki/Flash_memory

[10]
Information on principle SRAM memory implementation and related functionality, 2009, http://www.cedcc.psu.edu/khanjan/vssram.htm

[11]
IC Knowledge LLC, IC Cost Model, 2008, revision 0808,

[12]
Deliverable D5.6.2, 'Microcontroller with Integrated DSP and SIMD Capability', SOCRADES, 2008/2009, EU-public funded project.

### *5.2. Related standards and norms*

- None -

# 6. Acronyms and Abbreviations

| *Abbreviation / Acronym:* | *Description:* |
|---|---|
| ECU/MCU | Microcontroller (Unit) |
| SIMD | Single Instruction Multiple Data |
| RISC | Reduced Instruction Set Computer |
| ETM | Embedded Trace Macro cell |
| NVIC | Nested Vector Interrupt Controller |
| WIC | Wake-up Interrupt Controller |
| DAP | Debug Access Port |
| DSP | Digital Signal Processor / Processing |
| IP | Intellectual Property |
| CPU | Central Processing Unit |
| I/O | Input/Output Interface |
| die | Piece of silicon which realizes the required MCU functionality without package |

**Table 2: Acronyms & Abbreviations**

As this is a document from professionals for professionals, all other terms are expected to be known.

# 7. Annex A – Dissemination Levels

| | |
|---|---|
| PU | Public |
| PP | Restricted to other programme participants (including the Commission Services) |
| RE | Restricted to a group specified by the consortium (including the Commission Services) |
| CO | Confidential, only for members of the consortium (including the Commission Services) |

**Table 3: Dissemination levels for a document**